Notice of Allowability	Application No.	Applicant(s)
	10/681,566	MARTINEZ ET AL.
	Examiner	Art Unit
	Mark A. Osele	1734
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>RCE filed September 26, 2006</u> .		
2. The allowed claim(s) is/are <u>23-44</u> .		
3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)		
Attachment(s) 1. Notice of References Cited (PTO-892) 2. Notice of Draftperson's Patent Drawing Review (PTO-948) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material		(PTO-413), e

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EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Allan Fanucci on December 5, 2006.

The application has been amended as follows:

In the claims:

- 29. (Currently Amended) The method of claim 28 wherein the notch is annular and further comprising attacking the substrate at a third location with a third cutting blade, wherein the first, second and third cutting blades are arranged symmetrically about the annular notch of the semiconductor substrate.
- 30. (Currently Amended) An automatic high-precision cutting method for separating a layer of material from a source substrate comprising:

providing a semiconductor substrate having a weakened area, a sidewall and a notch in the sidewall, wherein the notch is positioned away from the weakened area;

positioning at least a portion of the sidewall of the semiconductor substrate against a fixed positioning member while supporting the substrate on a support;

contacting at least one blade with the notch of the semiconductor substrate to induce a cleaving wave into the substrate, the cleaving wave being of sufficient intensity to both divide the substrate at the notch into first and second parts and detach the layer from the substrate along the weakened area; and

moving at least a portion of the support away from the substrate as the blade contacts the notch so that the positioning member and blade are the only structures supporting the substrate.

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- 32. (Currently Amended) The method of claim [[23]] <u>30</u> wherein the positioning member is at least one shim oriented vertically with respect to the support and the support is a support substrate that is operatively associated with the positioning member so that the positioning member maintains the position of the semiconductor substrate in a cutting plane that is parallel to the at least one blade and the support member.
- 33. (Currently Amended) The method of claim [[23]] 32 wherein the shim has a contour that corresponds to the contour of the semiconductor substrate and covers at least one quarter of the periphery of the substrate to hold the wafer when contacted by the blade and the at least one blade has a leading edge that has a contour that corresponds to the contour of the semiconductor substrate and covers at least one quarter of the periphery of the substrate.
- 34. (Currently Amended) An automatic high-precision cutting method for separating a layer of material from a source substrate comprising:

providing a semiconductor substrate with a first face, a second face, a side surface and a notch in the sidewall side surface;

forming a weakened area in the semiconductor substrate which is located a distance from the notch;

providing a fixed positioning member adjacent a first support;

positioning at least a portion of the side surface of the a semiconductor substrate on the <u>first</u> support and against the positioning member; and

contacting the substrate with at least one blade to induce a cleaving wave into the substrate, the cleaving wave being of sufficient intensity to both divide the substrate at the notch into upper and lower parts and detach the layer from the substrate along the weakened area without limiting upward movement of the upper part of the wafer during cleaving,

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wherein the positioning member prevents movement of the substrate as the blade contacts the substrate, and

wherein the substrate is held in position between the positioning member and the blade without any support contacting the first and second faces.

- 40. (Currently Amended) The method of claim 39 wherein the notch is annular and further comprising attacking the substrate at a third location with a third cutting blade, wherein the first, second and third cutting blades are arranged symmetrically about the annular notch of the semiconductor substrate.
- 41. (Currently Amended) The method of claim 34, which further comprises supporting the substrate on a <u>second</u> support prior to contact by the at least one blade and moving the <u>second</u> support away from the substrate as the blade contacts the annular notch.
- 42. (Currently Amended) The method of claim 34 which further comprises viewing the progress of the cleaving wave with a sensor through a transparent window located in the <u>first</u> support.
- 43. (Currently Amended) The method of claim [[34]] <u>41</u> wherein the positioning member is at least one shim oriented vertically with respect to the <u>second</u> support and the <u>second</u> support is a support substrate that is operatively associated with the positioning member so that the positioning member maintains the position of the semiconductor substrate in a cutting plane that is parallel to the at least one blade and the <u>first</u> support-member.

The following is an examiner's statement of reasons for allowance: None of the prior art, either alone or in combination, suggest forming a cleave in a substrate wherein

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the substrate is only supported along its side surface thereby being unsupported at its upper and lower faces. The newly cited reference to Yanagita et al. '959 shows supporting the substrate at the side surface only but this occurs only during the second separating stage. During formation of the original cleave, the substrate is supported at its lower face so it can be rotated.

The newly cited references to Yanagita et al. '553 and Naruoka et al. '242 each show separating a substrate wherein the substrate is supported along its side surface and partially along the upper or lower face as well.

The previously cited reference to Laporte suggests supporting the substrate along its lower face as it is contacted by separating members at two locations along its annular side surface.

References to Rayssac et al. '649, Park et al. '435, and Tomita '697 show supporting substrates along their side surfaces, but the references are not prior art against the instant application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Osele whose telephone number is 571-272-1235. The examiner can normally be reached on M-F 9:30-6:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christopher Fiorilla can be reached on 571-272-1187. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MARK A. OSELE PRIMARY EXAMINER

December 8, 2006